SPECIFICATIONS
Models 1878/1879
96 CHANNEL PIPELINE TDC

Inputs:	96 ECL differential line receivers. Input impedance 110 Ω ± 10%. Minimum pulse width 10 nsec fwhm (must be >1 time bin width). Input swing ⩾400 mV, differential.
Phase Latch Accuracy:	± 200 psec or ± 10% of time bin size, whichever is greater
Least Count	
(Phase Latch):	
Model 1878	2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31.5 nsec with Model 1810 (half time bin size).
Model 1879	1, 2, 4 or 8 nsec, CSR selected in stand alone mode. 1 to 15.5 nsec with Model 1810 (half time bin size).
(Time Bin Size):	
Model 1878	4, 8, 16 or 32 nsec, CSR selected in stand alone mode. 4 to 63 nsec with Model 1810.
Model 1879	2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31 nsec with Model 1810.
TDC Range:	
Model 1878	9 bits, 8 + Phase Latch
Model 1879	10 bits, 9 + Phase Latch
Long Term Stability:	± 0.02 %
Full Scale:	1, 2, 4 or 8 μsec, ± 0.01%, CSR selected in stand alone mode. 1 to 16 μsec with 1810.
Double Pulse Resolution:	3-15 bins programmable, Compacting Mode. 3 bins, "All True Data" Mode.
Common Stop Trigger:	From the Model 1810 CAT Module via TR line or from front panel differential ECL input. CSR selected.
Sync Input:	Differential ECL two pin input. Terminated in 100 Ω Minimum width 10 nsec. Quenches the Acquisition Oscillator for the duration of the input width. Acquisition Oscillator is active and stable after a time equal to 4 times the Sync pulse width. Synchronism is achieved with respect to the trailing edge of the Sync pulse. Sync accuracy: 0.1 time bins at start up. See Long Term Stability spec above. Recommended width: (8 ± ½)/f. Here f is the Acquisition Oscillator frequency, i.e., input to the divide down circuit.
Channel-to-Channel Matching:	
Gain:	< ± 0.01% card-to-card
Pedestal:	< ± 4 nsec channel-to-channel
Differential Non-Linearity:	<1 nsec, typical
Integral Non-Linearity:	< ± 0.5 nsec or ± 0.25 LSB, whichever is greater
Pedestal Stability:	<100 psec/°C, 1 nsec long term
Fast Clear Response Time:	<10 nsec. Must be performed during MPI. 50 nsec minimum width
AS-AK Handshake Time:	30 nsec, typical
DS-DK Handshake Time:	80 nsec, typical
Digital Clear:	1.6 μsec
Conversion Time:	412 μsec + approximately 50 nsec per hit

GENERAL

Power Requirements:	5 mA at 15 V 7.2 A at +5 V (Model 1879, 8.5 A) 4.2 A at −5.2 V 2.0 A at −2 V (Model 1879, 3.3 A) 50 mA at −15 V
Packaging:	Single width FASTBUS module in conformance with FASTBUS Specification dated December, 1983.

FASTBUS CONTROL

Implemented Addressing Modes: Geographical, Secondary, Broadcast

Implemented Broadcast Functions:

Code	Significance	Comments
$(01)_h$*	General Broadcast Select	The TDC modules are selected and respond to subsequent data cycles.
$(09)_h$	Sparse Data Scan (SDS)	TDC modules containing time data assert their "T pin" on the following read data cycle.
$(09)_h$	Pattern Select	TDC's seeing their T pin asserted on the following write data cycle become selected to respond to subsequent data cycles.
$(0D)_h$	All Device Scan	All TDC modules assert their T pin on the following read data cycle.
$(AD)_h$	TDC SDS	Unique sparse data scan for only 1878 and 1879 modules. Follows standard SDS (see above).
$(BD)_h$	AFC SDS	All TDC modules with AFC's requiring service assert their T pins.

Slave Status Responses to Data Cycles:

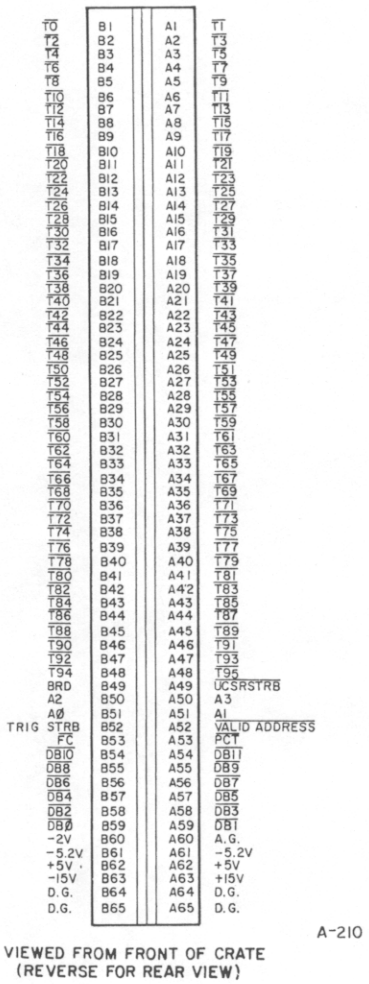
SS	Significance
0	Valid action.
1	Busy. The module is in the encoding mode and will not respond to data space read or write transactions.
3	Valid data space read with second event pending encoding.
2	End of data
6	Error. Non-implemented secondary address or invalid mode.
7	Error. Invalid secondary address loaded into internal address register.

*An h subscript denotes a hexadecimal number, i.e., base 16.

CONTROL FUNCTIONS IMPLEMENTED
(CSR Space)

Module Identification Code:	Read Only $(1032)_h$ for 1878, $(1033)_h$ for 1879.
Compacting Parameters (Z):	A 4-bit programmable number of leading zeros which must precede a 0 to 1 transition to be recognized as a hit. To account for edge effects, all history before the first time bin is assumed equal (0 or 1) to the first bin. To allow a diagnosis of "stuck" channels, first bin reporting may be enabled via "Enable Bin 1" of CSR0. All True Data mode (Z = 0) reports every true bin.
Readout Depth, active time interval (ATI):	A 5-bit programmable time range for valid data. For 1878, the number of valid time bins is 8(ATI + 1). For 1879, 16(ATI + 1). The valid bins are those corresponding to the earliest times.
Calibration Enable (T_e and T_o):	Two bits enable the TDC to receive the test input via a TR line and apply it to the even and odd TDC channels, respectively.
Common Stop Source:	Selects the source of the Common Stop, either front panel or a TR line.
FREF Source:	Selects either the internal crystal frequency reference or a rear panel low frequency reference, via a TR line (normally supplied from the CAT).
Gain Control:	A 2-bit parameter used to divide down the on board shift register oscillator. The divide down factor is 1, 2, 4 or 8.
Reread:	Resets the memory pointers for event reread.
Stop Inhibit:	Used for disabling the TDC.
Encoding Inhibit:	Used to allow for two event buffering (one in SOS shift registers, one in data memory. If a second event is buffered, SS = 3 responses replace SS = 0 on valid data space reads.
AFC:	Fourteen locations allocated to Auxiliary Functions Card.

AUXILIARY CONNECTOR
(Auxiliary Functions Card Socket)



A-210

VIEWED FROM FRONT OF CRATE
(REVERSE FOR REAR VIEW)

Hit Pulses:	96 signals called $\overline{T0}$ to $\overline{TR95}$. Pulse equal in duration to the front panel input pulse duration. TTL, active low signals.
Trigger Strobe:	A signal received by the TDC via the FASTBUS segment from the 1810 CAT module. Normally used by the AFC to define the fiducial time interval.
$\overline{DB0}$-$\overline{DB13}$:	A 14-bit bidirectional bus. TTL, active low.
BRD:	Defines direction of data bus $\overline{DB0}$-$\overline{DB13}$. When high AFC is in read mode (i.e., being read from the Segment).
Address Lines:	A0-A3; $\overline{UCSRSTRB}$: Addresses A0-A3 in conjunction with the decode AFC address strobe ($\overline{UCSRSTRB}$) allows user implementation of FASTBUS CSR locations $C0000002_h$ to $C000000F_h$. Fourteen locations are available for use on the AFC. A0-A3 are latched on TDC card.
$\overline{\text{Valid Address}}$:	TTL Active low signal to be driven by AFC circuits if an implemented address being accessed on the AFC. Used to generate the proper SS = 0 response to FASTBUS; otherwise, SS = 6 is generated if $\overline{\text{Valid Address}}$ is not driven low.
Power Supply:	All FASTBUS voltages.
$\overline{PCT}$:	TTL active low signal asserts module t pin (Service Request) in response to a $(BD)_h$ broadcast.
$\overline{FC}$:	TTL active low signal equal in duration to the Fast Clear input applied via the front panel or 1810 CAT module.